■ DESCRIPTION

The T68K1M, T68S1M, and T68R1M device family is a low power and high performance CMOS SRAM organized as 131,072 words by 8 bits. It operates from 2.7V to 3.6V, 2.2V to 2.7V, and 1.65V to 2.2V. Easy memory expansion is provided by an active LOW chip enable 1 (/CE1), active HIGH chp enable 2 (CE2) and active LOW output enable (/OE) and three-state I/O drivers. Four control pins (/CE1, CE2, /OE, and /WE) fully control the operation mode of the T68 K/S/R 1M device family. An active LOW write enable signal (/WE active low) controls the write/read operation of the memory. When /CE1 and /WE inputs go LOW and CE2 input goes HIGH simultaneously, the device is in write mode and data on the 8 data pins (IO1~IO8) is written into the memory location specified by the address on address pins (A0~A16). When /CE1 and /OE inputs go LOW and CE2 and /WE input stay in HIGH state, the device is in read mode and data in the specified memory address is driven onto the 8 data pins. The 8 data pins will be in high-impedance state if both /OE and /WE pins are in HIGH (inactive) state. The T68 K/S/R 1M device family has an automatically power-down feature when the chip is deselected (/CE1 pin HIGH or CE2 pin LOW). The T68 K/S/R 1M device family is available in JEDEC standard 32-pin 450-mil SOP, 32-pin 8mmx20mm plastic TSOP, 32-pin 8mmx13.4mm plastic STSOP, and 36-ball 6mmx8mm BGA package, also for DICE.

■ FEATURES

- Operation voltage……T68K1M……2.7V ~ 3.6V
  T68S1M…… 2.2V ~ 2.7V
  T68R1M…… 1.65V ~ 2.2V
- Low active power and standby power
- High access times: 70ns/85ns/100ns
- TTL-compatible inputs and outputs
- Easy memory expansion with /CE1, CE2 and /OE
- Low data retention voltage……2.0V (for K), 1.5V (for S), 1.0V (for R)
- Auto power down when deselected

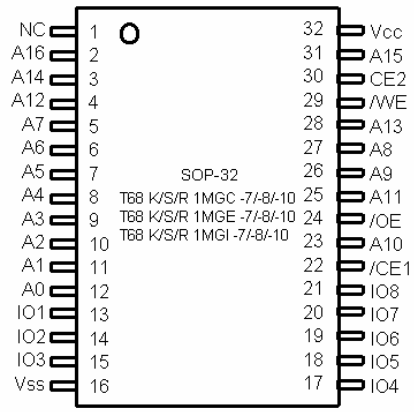
■ PRODUCT FAMILY

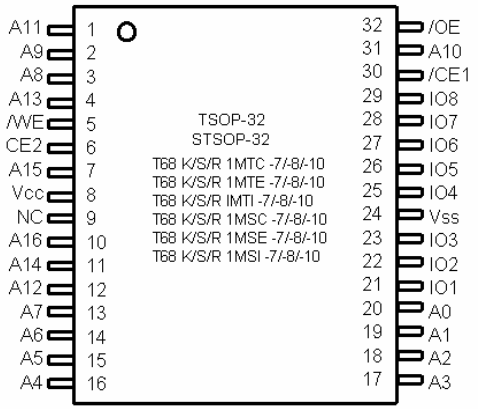
Part Number	V_{CC} Range	Speed	Operating Temperature	Power Dissipation		Package Type
				Operating (I_{CC2}, Max.)	Standby (I_{SB1}, Max.)	
T68K1MGC -7/-8	2.7V~3.6V	70ns/ 85ns	Commercial (+0°C~+70°C)	20mA	3uA	SOP-32
T68K1MTC -7/-8						TSOP-32
T68K1MSC -7/-8						STSOP-32
T68K1MBC -7/-8						BGA-36
T68K1MDC -7/-8						Dice
T68S1MGC -7/-8	2.2V~2.7V			20mA	3uA	SOP-32
T68S1MTC -7/-8						TSOP-32
T68S1MSC -7/-8						STSOP-32
T68S1MBC -7/-8						BGA-36
T68S1MDC -7/-8						Dice
T68R1MGC -8/-10	1.65V~2.2V	85ns/ 100ns		15mA	2uA	SOP-32
T68R1MTC -8/-10						TSOP-32
T68R1MSC -8/-10						STSOP-32
T68R1MBC -8/-10						BGA-36
T68R1MDC -8/-10						Dice

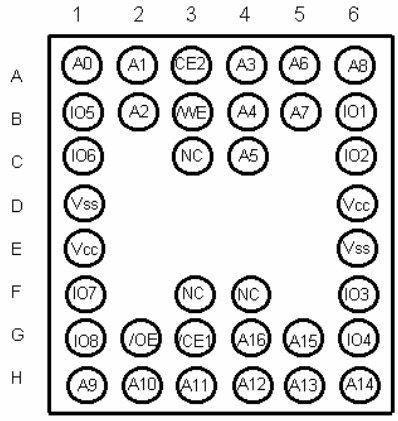
Part Number	V_{CC} Range	Speed	Operating Temperature	Power Dissipation		Package Type
				Operating (I_{CC2}, Max.)	Standby (I_{SB1}, Max.)	
T68K1MGE -7/-8	2.7V~3.6V	70ns/ 85ns	Extended (-25°C~+85°C)	20mA	3uA	SOP-32
T68K1MTE -7/-8						TSOP-32
T68K1MSE -7/-8						STSOP-32
T68K1MBE -7/-8						BGA-36
T68K1MDE -7/-8						Dice
T68S1MGE -7/-8	2.2V~2.7V			20mA	3uA	SOP-32
T68S1MTE -7/-8						TSOP-32
T68S1MSE -7/-8						STSOP-32
T68S1MBE -7/-8						BGA-36
T68S1MDE -7/-8						Dice
T68R1MGE -8/-10	1.65V~2.2V	85ns/ 100ns		15mA	2uA	SOP-32
T68R1MTE -8/-10						TSOP-32
T68R1MSE -8/-10						STSOP-32
T68R1MBE -8/-10						BGA-36
T68R1MDE -8/-10						Dice

Part Number	V_{CC} Range	Speed	Operating Temperature	Power Dissipation		Package Type
				Operating (I_{CC2}, Max.)	Standby (I_{SB1}, Max.)	
T68K1MGI -7/-8	2.7V~3.6V	70ns/ 85ns	Industrial (-40°C~+85°C)	20mA	3uA	SOP-32
T68K1MTI -7/-8						TSOP-32
68K1MSI -7/-8						STSOP-32
T68K1MBI -7/-8						BGA-36
T68K1MDI -7/-8						Dice
T68S1MGI -7/-8	2.2V~2.7V			20mA	3uA	SOP-32
T68S1MTI -7/-8						TSOP-32
T68S1MSI -7/-8						STSOP-32
T68S1MBI -7/-8						BGA-36
T68S1MDI -7/-8						Dice
T68R1MGI -8/-10	1.65V~2.2V	85ns/ 100ns		15mA	2uA	SOP-32
T68R1MTI -8/-10						TSOP-32
T68R1MSI -8/-10						STSOP-32
T68R1MBI -8/-10						BGA-36
T68R1MDI -8/-10						Dice

■ PIN CONFIGURATION



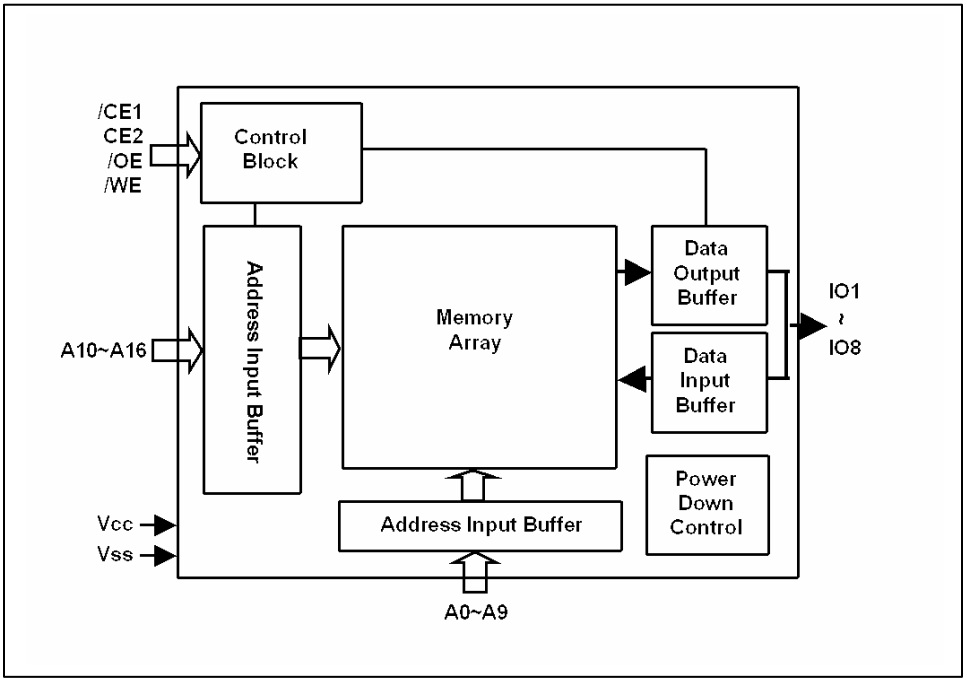




BGA-36 Top View (Ball Down)

T68 K/S/R 1MBC -7/-8/-10
T68 K/S/R 1MBE -7/-8/-10
T68 K/S/R 1MBI -7/-8/-10

■ LOGIC BLOCK



■ (PIN DESCRIPTION)

Pin Name	Function
A0 ~ A16	Address Input Pins
IO1 ~ IO8	Data Input/Output Pins
/CE1	Chip Enable 1 Input Pin
CE2	Chip Enable 2 Input Pin
/OE	Output Enable Input Pin
/WE	Write Enable Input Pin
V_{CC}	Power Supply Pin
V_{SS}	Ground Pin

■ TRUTH TABLE

Mode	/CE1	CE2	/WE	/OE	I/O1~8	Power
Deselected	H	X(1)	X	X	High-Z	Standby
Deselected	X	L	X	X	High-Z	Standby
Write	L	H	L	X	Input	Active
Read	L	H	H	L	Output	Active
Output Disabled	L	H	H	H	High-Z	Active

1. ' X' means don' t care. Must be in high or low state.

■ ABSOLUTE MAXINUM RATINGS (1)

Symbol	Parameter		Rating	Unit
V_{CC}	Power Supply Voltage (to V_{SS})		-0.5 ~ Vcc.max+1V(2)	V
			-0.5 ~ Vcc.max+0.3V(3)	V
V_{IN}/V_{OUT}	Input / Output Voltage		-0.5 ~ Vcc+0.5V(2)	V
			-0.5 ~ Vcc+0.3V(3)	V
I_{OUT}	Output Current into Outputs (LOW)		20	mA
P_D	Power Dissipation		1.0	W
T_{STG}	Storage Temperature		-65 ~ +150	^{O}C
T_{SOLDER}	Soldering Temperature and Time		260 ^{O}C , 10sec (Lead Only)	
T_A	Operating Temperature	C-Grade	0 ~ 70	^{O}C
		E-Grade	-25 ~ 85	
		I-Grade	-40 ~ 85	

1. Stresses greater than those listed in the **Absolute Maximum Ratings** table may cause permanent damage to the device.Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.
2. For K and S family.
3. For R family.

■ RECOMMENDED DC OPERATING RANGE

Symbol		Parameter	Rating	Unit
V_{CC}	T68K1M	Supply Voltage	2.7 ~ 3.6	V
	T68S1M		2.2 ~ 2.7	V
	T68R1M		1.65 ~ 2.2	V
V_{SS}		Ground	0	V
V_{IH}	T68K1M	Input High Voltage	2.2 ~ V_{CC}+0.5	V
	T68S1M		2.0 ~ V_{CC}+0.5	V
	T68R1M		1.4 ~ V_{CC}+0.5	V
V_{IL}	T68K1M	Input Low Voltage	-0.5 ~ 0.6	V
	T68S1M		-0.5 ~ 0.6	V
	T68R1M		-0.5 ~ 0.4	V

■ CAPACITANCES (1)

Symbol	Parameter	Min.	Max.	Condition
C_{IN}	Input Capacitance	-	8pF	Unmeasured pins set to 0V
C_{IO}	Input/Output Capacitance	-	10pF	

1. The Capacitances listed in the above table are sampled, not 100% tested.

■ DATA RENTATION CHARACTERISTICS

Symbol	Parameter		Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	T68K1M	Standby Mode		2.0	-	3.6	V
		T68S1M			1.5	-	2.7	
		T68R1M			1.0	-	2.2	
I_{DR}	Data Retention Current	T68K1M	V_{CC}=2.0V and CMOS Standby mode(1)	C-Grade	-	-	2	uA
				E-Grade	-	-	3	
				I-Grade	-	-	3	
		T68S1M	V_{CC}=1.5V and CMOS Standby mode(1)	C-Grade	-	-	1	
				E-Grade	-	-	2	
				I-Grade	-	-	2	
		T68R1M	V_{CC}=1.0V and CMOS Standby mode(1)	C-Grade	-	-	1	
				E-Grade	-	-	2	
				I-Grade	-	-	2	
T_{SDR}	Data Retention Setup Time		See data retention waveform		0	-	-	ns
T_{RDR}	Data Retention Recovery Time				T_{RC}	-	-	ns

Note: 1. Standby mode: /CE1≥Vcc-0.2V or CE2≤ Vss+0.2V

■ DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current		V_{IN} = V_{SS} to V_{CC}	-1	-	1	µA
I_{LO}	Output Leakage Current		/CE1=V_{IH} CE2=V_{IL} or /OE=V_{IH} or /WE=V_{IL}, V_{IO}=V_{SS} to V_{CC}	-1	-	1	µA
I_{CC1}	Average Operating Current	T68K1M	/CE1≤0.2V, CE2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V Cycle time = 1µs, 100%duty, I_{IO}=0mA	-	3(1)	6	mA
		T68S1M		-	3(1)	6	
		T68R1M		-	2(1)	4	
I_{CC2}		T68K1M	/CE1=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IN}=V_{IL}, Cycle time = min, 100% duty, I_{IO}=0mA	-	15(1)	20	mA
		T68S1M		-	15(1)	20	
		T68R1M		-	10(1)	15	
V_{OL}	Output Low Voltage	T68K1M	IOL = 2.0mA	-	-	0.4	V
		T68S1M	IOL = 0.5mA	-	-	0.4	
		T68R1M	IOL = 0.2mA	-	-	0.4	
V_{OH}	Output High Voltage	T68K1M	IOH = -1.0mA	2.2	-	-	V
		T68S1M	IOH = -0.5mA	2.0	-	-	
		T68R1M	IOH = -0.1mA	1.4	-	-	
I_{SB}	TTL Standby Current	T68K1M	/CE1=V_{IH} or CE2= V_{IL}, other inputs = V_{IH} or V_{IL}	-	-	0.2	mA
		T68S1M		-	-	0.2	
		T68R1M		-	-	0.2	
I_{SB1}	CMOS Standby Current	T68K1M	/CE1≥V_{CC}-0.2V or CE2≤V_{SS}+0.2V , other inputs = 0 to V_{CC}	-	1.0(1)	3	µA
		T68S1M		-	1.0(1)	3	
		T68R1M		-	0.8(1)	2	

Note: 1. Ta=25°C, V_{CC}=3.0V (K), V_{CC}=2.5V (S), and V_{CC}=1.8V (R), not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS

● TEST CONDITIONS

Input Pulse Level: 0.2Vcc($\leqq V_{IL}$), 0.8Vcc($\geqq V_{IH}$)

Input Rising and Falling Time: 5ns

Input and Output Reference Voltage: 0.9V(R), 1.1V(S), 1.5V (K)

Output Load: C_L = 30pF + one TTL gate

● READ CYCLE

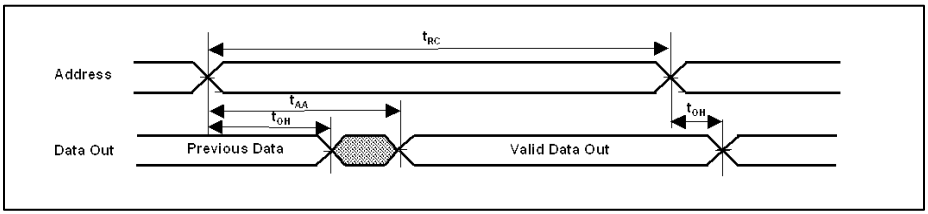
Symbol	Parameter List	Speed Bin						Units
		-7 (70ns)		-8(85ns)		-10(100ns)		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	70	-	85	-	100	-	ns
t_{AA}	Address Access Time	-	70	-	85	-	100	ns
t_{CO}	Chip Select to Output	-	70	-	85	-	100	ns
t_{OE}	Output Enable to Valid Output	-	35	-	40	-	50	ns
t_{LZ}	Chip Select to Low-Z Output	10	-	10	-	10	-	ns
t_{OLZ}	Output Enable to Low-Z Output	5	-	5	-	5	-	ns
t_{HZ}	Chip Disable to High-Z Output	0	25	0	25	0	30	ns
t_{OHZ}	Output Disable to High-Z Output	0	25		25		30	ns
t_{OH}	Output Hold From Address	10	-	10	-	15	-	ns

● WRITE CYCLE

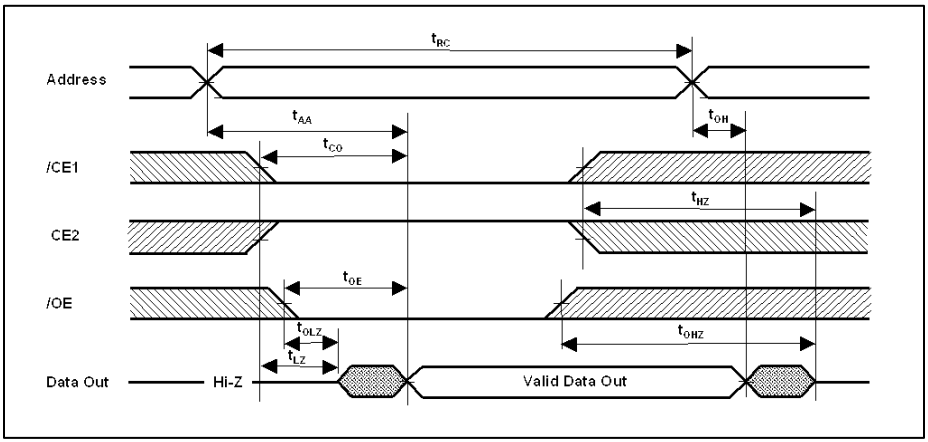
Symbol	Parameter List	Speed Bin						Units
		-7 (70ns)		-8(85ns)		-10 (100ns)		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t_{CW}	Chip Select to End of Write	60	-	70	-	80	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	60	-	70	-	80	-	ns
t_{WP}	Write Pulse Width	55	-	60	-	70	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output High-Z	0	25	0	25	0	30	ns
t_{DW}	Data to Write Time Overlap	30	-	35	-	40	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	End Write to Output Low-Z	5	-	5	-	5	-	ns

■ TIMING DIAGRAMS

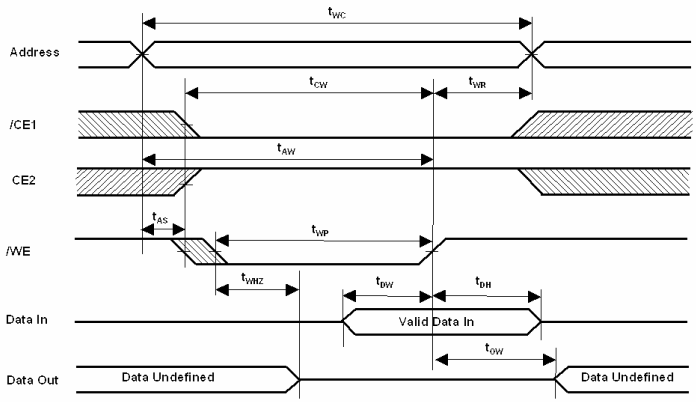
● TIMEING WAVEFORM OF READ CYCLE (1)
(Address Controlled, /CE1=/OE=VIL, CE2=/WE=VIH)



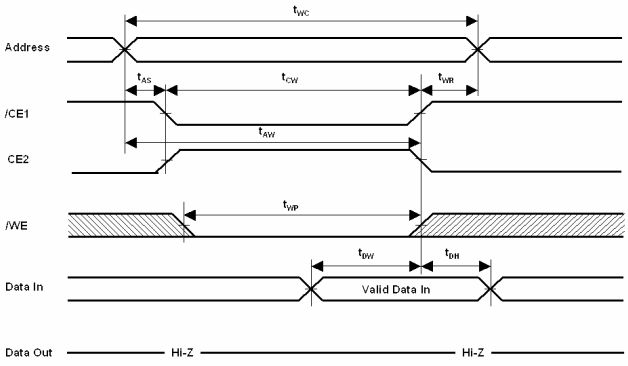
● TIMEING WAVEFORM OF READ CYCLE (2) (/WE=VIH)



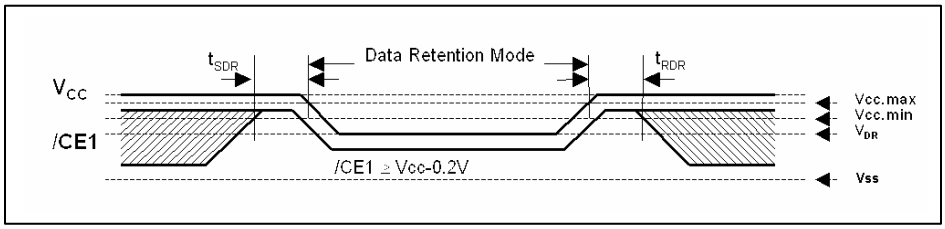
● TIMING WAVEFORM OF WRITE CYCLE (1) (/WE Controlled)



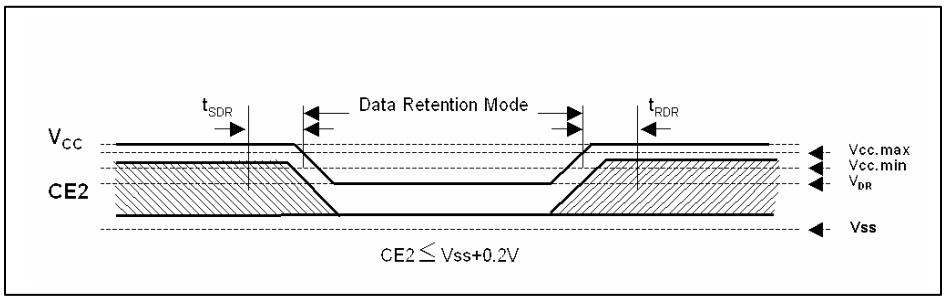
● TIMING WAVEFORM OF WRITE CYCLE (2) (/CE1 OR CE2 Controlled)



- **DATA RETENTION WAVEFORM (1) (/CE1 Controlled)**

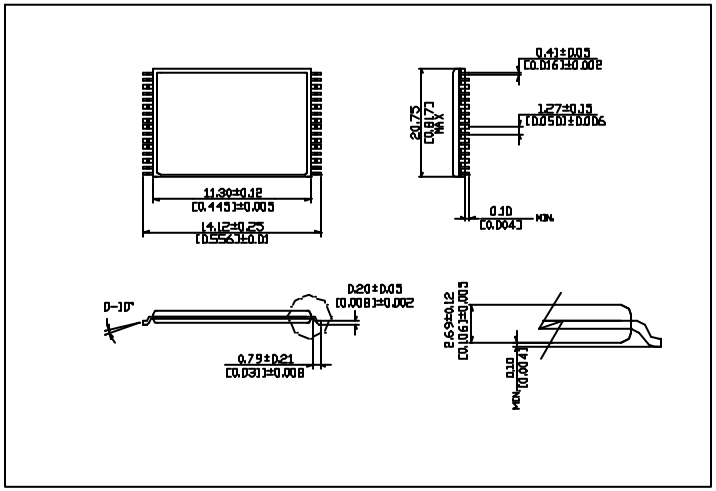


- **DATA RETENTION WAVEFORM (2) (CE2 Controlled)**

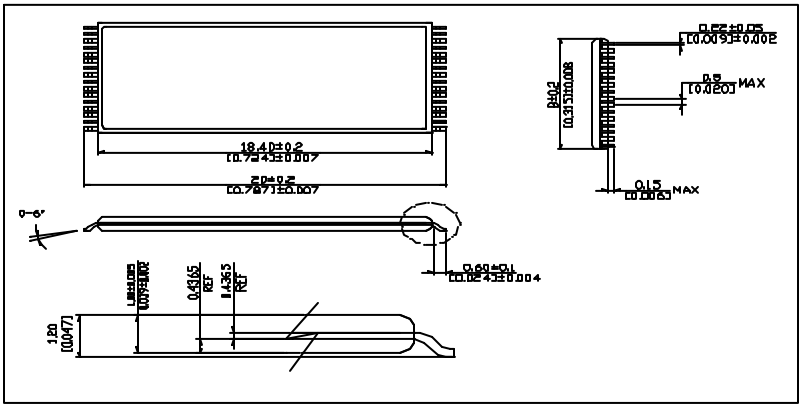


■ PACKAGE DIMENSION

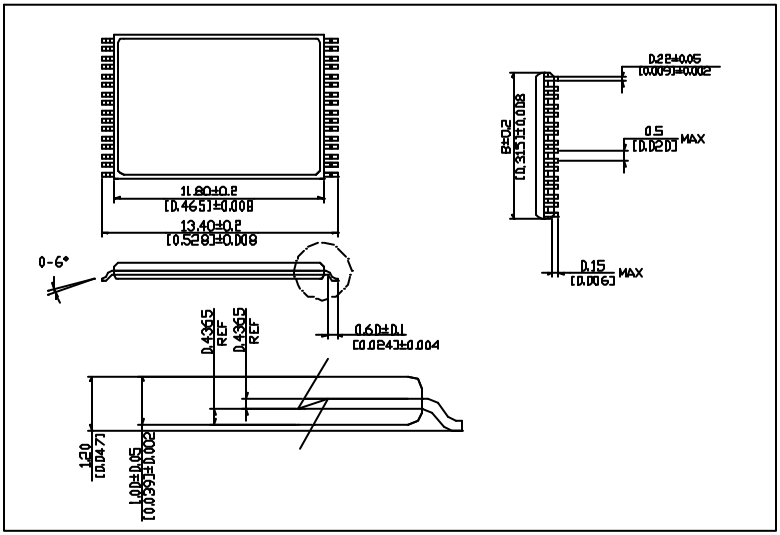
32L PIN SOP (445 mil)



32L PIN TSOP (8x20)



32L PIN TSOP (8x13.4)



36 BALL BGA (6mm x 8mm)